A MONOLITHIC MIXER IC: DESIGN AND CHARACTERISTICS ON N-IMPLANT ONLY, BURIED P-AND MBE WAFERS.

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ABSTRACT:

A monolithic high performance MESFET mixer integrated circuit has been developed for general purpose applications. In order to achieve high dynamic range, low power consumption and small size, active circuit techniques have been utilized for applications up to 4 GHz. The balanced mixer, which consists of active phase splitting networks and commutator cell was fabricated on different wafers having N-implant only, Buried P-layer and Molecular Beam Epitaxy. The monolithic integrated circuit has shown a conversion gain of 1 dB with RF and LO rejections greater than 20 dB, up to 4 GHz. A detailed comparison of the performance of the IC on different wafers is presented.

INTRODUCTION:

For system applications, Gallium Arsenide monolithic integrated circuits promise high volume, small size and low cost. Each application has its own special requirements such as dynamic range, size, cost, power consumption, packaging, etc. This paper reports the development of a GaAs monolithic MESFET mixer IC arrived for general purpose applications, both military and commercial, up to 4 GHz. A key feature of the IC design is the implementation of the active circuit techniques to realize small size phase splitting networks. In addition to the circuit design, the IC was fabricated on three different types of wafers. The wafers include N-implant only, N-implant with a buried P-layer and an MBE wafer using a step doping profile. Figure 1 shows the DC characteristics of the different wafers and indicates sharp pinch-off voltage obtained for buried p-wafer and a lower pinch-off voltage obtained for MBE wafers. A lower pinch-off voltage is ideal for mixer operation requiring low local oscillator power and a sharp pinch-off voltage is ideal for mixer operation in the switching mode.

MMIC DESIGN:

Figure 2 shows the block diagram of the balanced mixer. It consists of two active baluns [phase splitters] to provide the 0° and 180° inputs that are required to drive the MESFETS in the commutator mixer cell. The active phase splitting can be achieved in different manners as shown in Figure 3. The design approach used here implemented the common source, common gate approach which is similar to the differential amplifier configuration. The common source circuit provides phase inversion and a common gate circuit provides no phase inversion. Since the gain of the common source and common gate amplifiers is different, the device size was changed to compensate such that amplitude balance is maintained. The amplitude balance maintaining together with differential phase of 180° is necessary to achieve good RF and LO rejections at the intermediate, IF, port.

The mixer circuit is comprised of three main sections, namely, two phase splitters or baluns providing equal amplitude antiphase signals for the signal and local oscillator inputs and a commutator circuit for performing the frequency conversion. A single gate GaAs MESFET was chosen for the active devices. Dual-gate FETs could have been used to implement this commutator but experience has shown that there is poor isolation between the gate fingers, as low as 10 dB, when realized in the interdigitated form.

The circuit that performs the frequency conversion process is the commutator. This circuit essentially comprises two RF amplifiers that are alternatively switched into operation but ideally only one functions as an amplifier at any time. The alternate switching of these amplifiers is achieved by an LO signal at the gates of upper FETs, ideally, of equal magnitude and in antiphase. When the antiphase LO signals are applied to the gates of the two FETs, in series with the two devices acting as RF amplifiers, the two amplifiers are alternatively turned on and off by the LO.

The signal balun is virtually identical in design to

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the LO balun. Although, at any instant in time, a signal appears at both outputs of the signal balun, only one is amplified via the commutator at any one time. The output from the two amplifiers in the commutator are combined in phase to form an IF signal. It can, therefore, be seen that under ideal conditions, the output signal from the commutator will come first from the 0° output from the signal balun and then from the 180° output. In this mixer design, the rate of commutation is determined by the local oscillator frequency. The mixer cell is shown in Figure 4 and consists of four half micron MESFETs with gate widths of 200 μm to 250 μm. The mixer IC operates from a positive supply of five volts which is varied to achieve maximum conversion efficiency.

FABRICATION PROCESS:

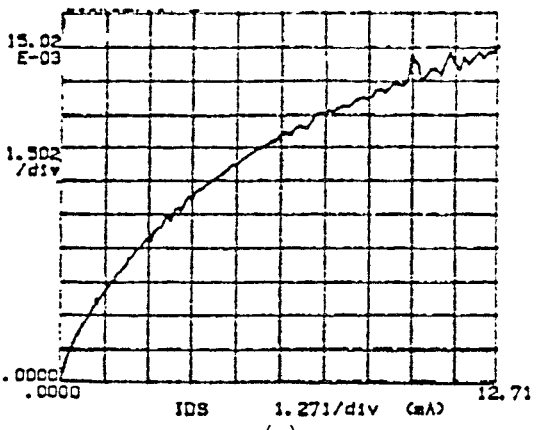
The MMIC fabrication starts with three different types of wafers which have active layers made by (a) Si implantation only (b) Si and Be co-implantation to have buried -P-layer, and (c) MBE growth. For the cases of ion implantations, M/A-COM undoped LEC semi-insulating GaAs substrates were used. Activation was achieved by annealing the wafers for twenty minutes at 850°C under arsine over pressure. In the case of MBE wafers, a step-function doping profile as shown in Figure 5 was grown on 0.5 μm superlatice buffer layer. There is no localized N+ region for the ohmic contacts in order to simplify the fabrication process. The FET gate length is 0.5 μm formed by E-beam lithography. The device isolation was done by boron ion implantation for the planar process. The wafer is passivated with 0.15 μm thick silicon nitride which is also used as the capacitor dielectric. Only GaAs resistors are used in this circuit and the interconnections are made by the airbridges. The wafer is thinned to 100 μm. The completed IC measures 1.75 mm by 1 mm.

MEASUREMENTS:

The monolithic mixer was mounted in an eight lead flat-pak package and measurements conducted to 5 GHz. The mixer provided a conversion gain of 1 dB to 4 GHz as shown in Figure 6. It has an output compression of 1 dB at an input power of 3 dBm, as shown in Figure 7. Typical RF and LO rejections of the order of 15 dB to 20 dB below the signals have been detected at the IF ports as shown in Figure 8. This could be improved substantially by RF decoupling the supplies of the phase splitters near the die. The die photograph is shown in Figure 9. The complete comparison results will further be presented.

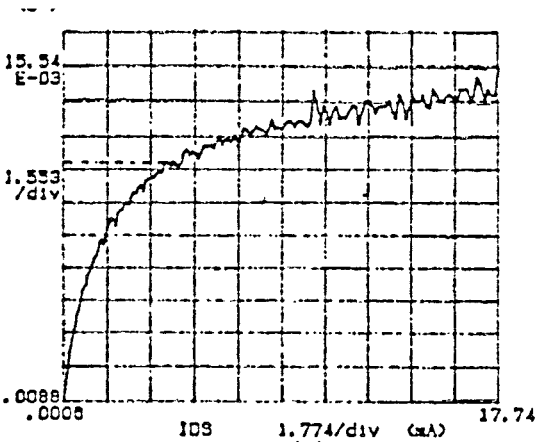
ACKNOWLEDGMENT

The authors would like to thank Dr. D. Maki for permission to publish this paper and for perpetuating the work.



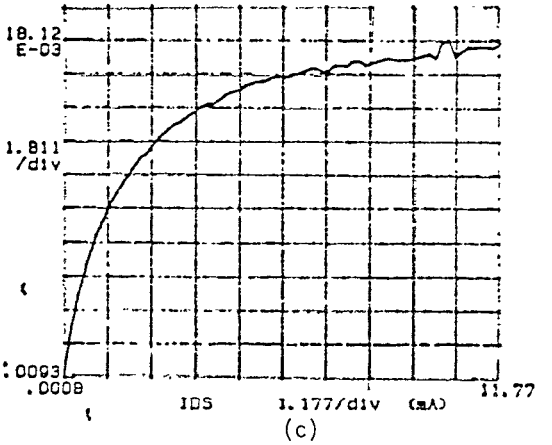
(a)

N-Implant



(b)

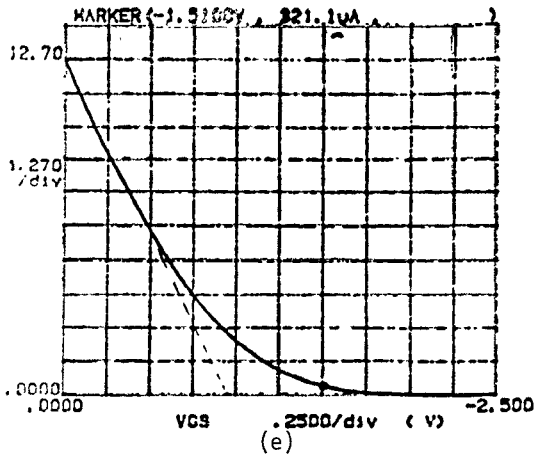
Buried P



(c)

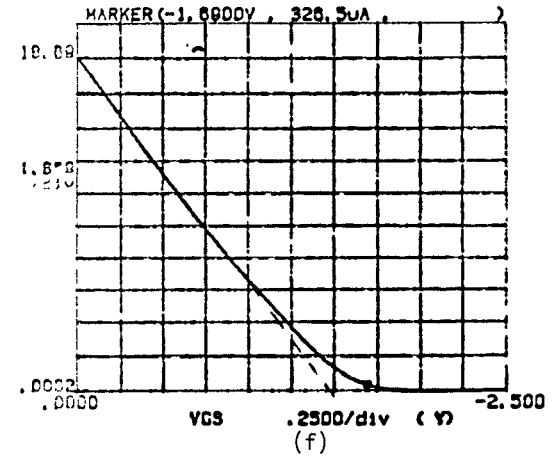
MBE

Figure 1 (a,b,c). Detail g_m vs I_{ds} for N-, buried P, and MBE wafers.



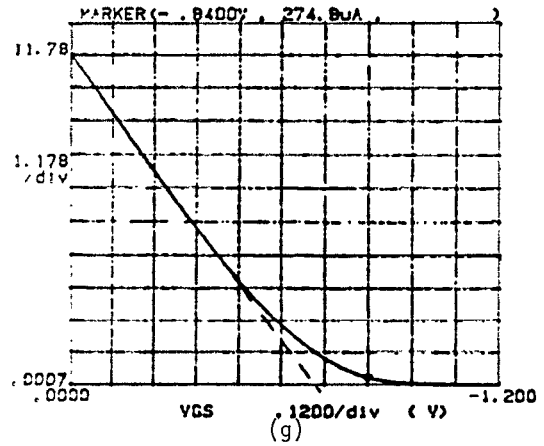
(e)

N-



(f)

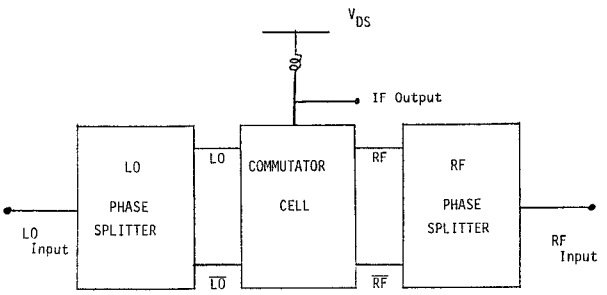
Buried P



(g)

MBE

Figure 1 (d,e,f). Detail the I_{ds} vs V_{gs} characteristics for N-, buried P, and MBE wafers.



RF AND LO CANCELLATION AT IF

Figure 2. Mixer Block Diagram.

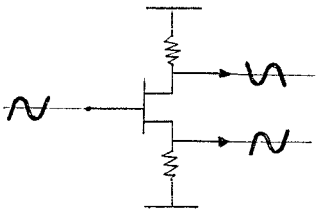


Figure 3(a). Single FET Phase Splitter

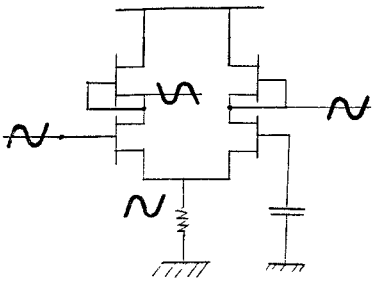


Figure 3(b). Differential Amplifier Phase Splitter

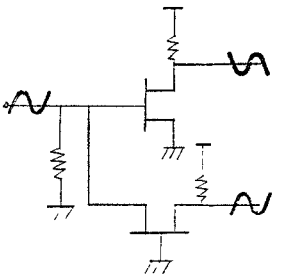


Figure 3(c). Common Source, Common Gate Phase Splitter

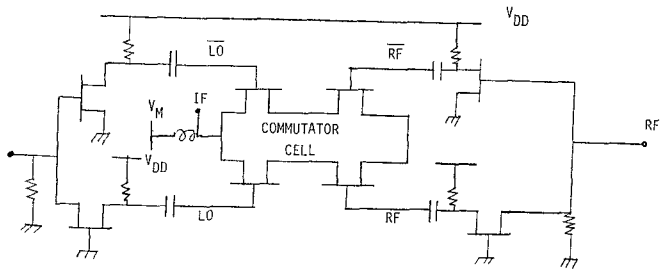


Figure 4. Mixer Schematic.

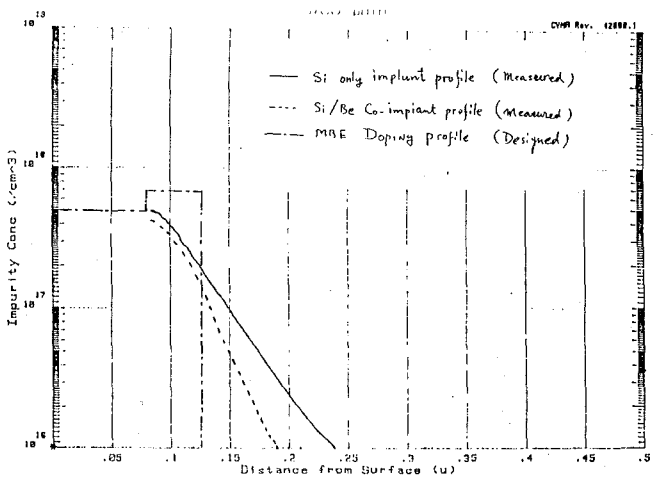


Fig 5

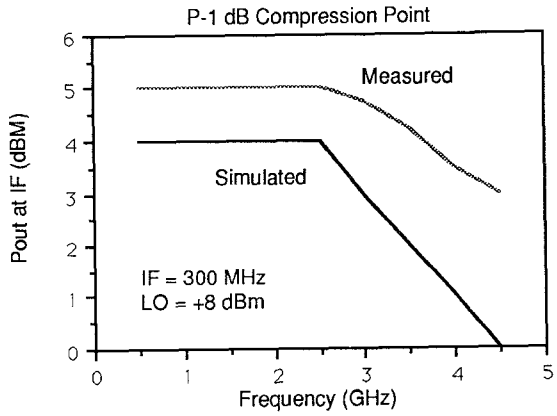


Fig 7

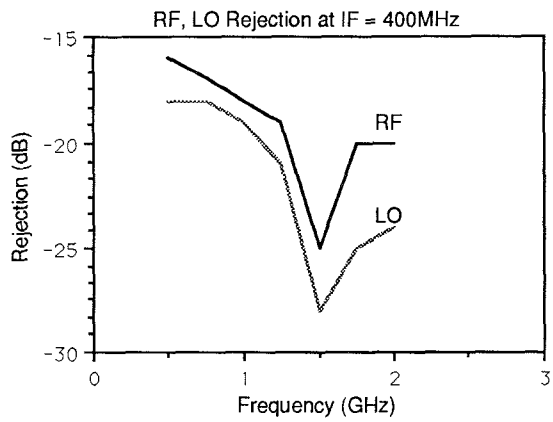


Fig 8

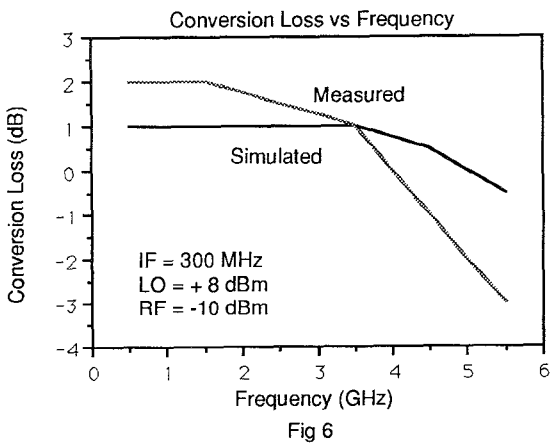


Fig 6

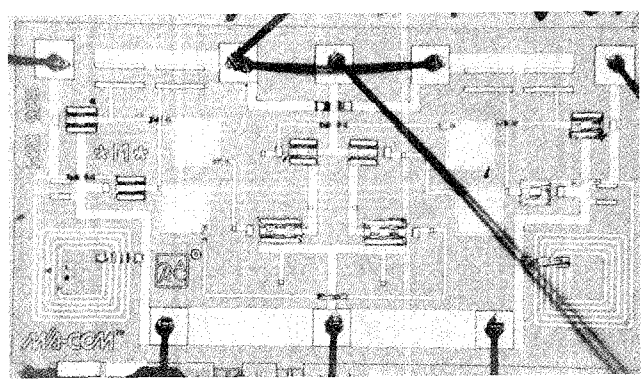


Fig 9